

### **REMARKS**

Applicants appreciate the thorough examination of the present application as evidenced by the Office Action. However, Applicants request withdrawal of the rejections for at least the reasons discussed below.

#### **The Drawing Objection:**

Figure 5 is objected to for failure to "clearly show the electrical connections of core outputs C2D1-C2DN of unit 539 with the corresponding input ports of MUX 531." Final Action, p. 4. An attached markup sheet was also provided by the Examiner. As an initial matter, Applicants agree the Examiner's markup sheet accurately reflects connections and, thus, is not objectionable to the Applicants. However, Applicants disagree that the additional lines are required on the drawing. In fact, to make the drawing clearer, rather than include the requested feedback lines, Figure 5 includes a common label for the signals C2Dx at the output of the second core logic circuit unit 539 and the input to the unit 520. Thus, Applicants submit that Figure 5 is clear without adding the lines requested by the Examiner. While the Applicants will submit a corrected drawing if the objection is not withdrawn (copy attached hereto), Applicants request that the Examiner withdraw the objection to avoid the expense of replacement drawings as Figure 5 is sufficiently clear as presently drawn.

#### **The Section 112 Rejections:**

Claims 1-24 stand rejected under 35 U.S.C. § 112, first paragraph, as failing to comply with the written description requirement. Final Action, p. 4. More particularly, the Final Action asserts that the specification of the present application fails to describe the "without synchronizing" language added to various claims by the Applicants' previous amendment.

The basis of this rejection is presented more extensively in the Response to Arguments section of the Final Action. Final Action, pp. 2-4. Based on those comments, it would appear that the Examiner has interpreted the "without synchronizing" language

as related to the internal operation of the multiplexer unit 520 and the flip-flop unit 535 of the scan test circuit unit 535. However, regardless of the accuracy of the Examiner's characterization of the operation of these circuits, as applied to the illustrated embodiments of Figure 5, the recitations added to the independent claims related to the signals as provided from the multiplexer unit 520 and the first core logic circuit unit 531.

For example, as recited in Claim 1, the multiplexer (MUX) unit "selectively provides the sub data or the core output data as inputs to the input ports of the core block, without synchronizing therebetween." Thus, "therebetween" refers to between the MUX unit and the input ports of the core block, not any operations within either the MUX unit or the core block.

As properly interpreted, the application as filed clearly meets the written description requirement. As an initial matter, the direct connection between units 520 and 531 in Figure 5, for example, clearly shows the recited arrangement. In addition, the background section discusses various prior art approaches where synchronously operated scan test circuits (Figures 2-4) are used around the core block, which approaches are described as disadvantageous in light of factors such as increased size of the device. See, Specification, p. 4, lines 19-24. More particularly, as discussed in the present specification, various prior art approaches require that each port of the core block be included in a peripheral scan test circuit. Specification, p. 2, line 16 to p. 3, line 4. Examples of such peripheral scan test circuitry, shown in Figures 2-4, include multiplexers as well as flip-flops to provide synchronization to a system clock. In contrast, as described in the present specification:

According to some embodiments of the present invention, when scan test circuits, whose number is the same as the number of input ports or output ports of a device, are included around a programmable intellectual property (IP) core, only one MUX may be needed for each port near an input terminal of the programmable IP core. Therefore, the scan test circuit may be simplified to allow chip downsizing.

Specification, p. 14, lines 16-20. Thus, the absence of such synchronizing is mentioned and distinguished in the application as filed, which Applicants submit clearly meets the written description requirement. Accordingly, Applicants request withdrawal of the

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Section 112 rejections.

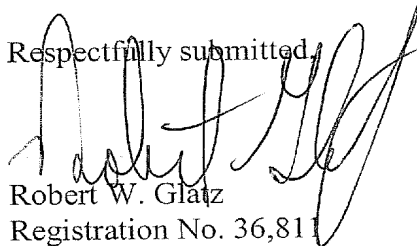
**The Section 102 Rejections:**

Claims 1-24 stand rejected under 35 U.S.C. § 102(b) as anticipated by United States Patent No. 5,774,476 to Pressly *et al.* ("Pressly"). Final Action, p. 5. Applicants note the Section 102 rejections appear to be unchanged from the previous Office Action. Accordingly, Applicants' previous responsive Amendment is incorporated herein as if set forth in its entirety rather than repeating those arguments herein. Applicants further note that, as the arguments are unchanged, they fail to address the "without synchronizing" recitations of the independent claims. Accordingly, the rejections should also be withdrawn at least as they fail to even address some of the recitations of the pending independent claims. The dependent claims are patentable at least based on the patentability of the claims from which they depend.

**CONCLUSION**

Applicants respectfully submit that the reference cited in the present rejections does not disclose or suggest the present invention as claimed and that the written description requirement is met for the reasons set out above. Accordingly, Applicants respectfully request reconsideration of the rejections by the Examiner and allowance of all the pending claims and passing this application to issue.

Respectfully submitted,



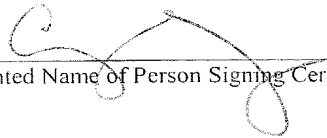
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